IN THE SPECIFICATION

Please amend specification as indicated below, the replacement paragraphs showing the changes with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing

On Page 2 of the specification, edit as follows:

Paragraph 1, line 1

a first section having a multi-bit analog to digital converter for receiving an analog input signal and generating an m-bit digital signal;

Paragraph 2, line 5

an m-bit to n-bit converter (where m>n) for receiving the m-bit digital signal and for generating an n-bit digital output signal for outputting across an interface, wherein the m-bit to n-bit converter quantizes the m-bit signal to a lower resolution[[.]]; and

a second section having processing means which is arranged to receive the n-bit digital signal and to process the received signal to generate an output digital signal.

Paragraph 3, line 7

The use of a multi-bit analog-to-digital converter, such as a multi-bit sigma-delta modulator, at the input stage (i.e., first section) increases the overall performance of the converter compared to the use of a single-bit converter. This is because higher performance is more easily achieved by a multi-bit (sigma-delta) modulator than a single-bit (sigma-delta) modulator.

Paragraph 4, line 13

The use of an m-bit to n-bit converter reduces the number of physical connections that are required for the interface to a second section of the converter, while maintaining good performance. Preferably, the m-bit to n-bit converter is an m-bit to single-bit converter as this ~~minimises~~minimizes the connection requirements of the interface. Preferably, the rate at which the m-bit signal is received at the converter is the same as the rate at which the n-bit output signal is generated. This allows all transfers in the first section of the converter to occur at the same clock rate, which reduces interference.

Paragraph 5, line 19

Preferably, a second section of the converter comprises an n-bit to p-bit converter for receiving the n-bit digital signal from the interface and for generating a p-bit digital signal (n<p) at a higher resolution and a filter which filters~~filtering means for filtering~~ the p-bit signal to generate a digital output. In this way a multi-bit signal can be recovered in the second section, if desired.

Paragraph 7, line 24

a first section having an input for receiving an s-bit digital signal from an interface and for generating a t-bit digital signal (where s<t) at a higher resolution; and

Paragraph 8, line 26

~~digital-to-analog conversion means for receiving the t-bit digital signal and generating an analog output.~~a digital-to-analog converter which receives the t-bit digital signal and generates an analog output; and

a second section connectable to said first section by said interface and having an input for receiving a digital signal, and a processor which receives the digital input signal and generates an s-bit digital output signal.

Paragraph 9, line 28 and 29

An input (i.e., first) section can be connected to the interface. The input section comprises an input for receiving a digital signal and an r-bit to s-bit converter (where r>s) for receiving ~~the~~an r-bit digital signal and for generating an s-bit output signal for outputting across the interface. The converter quantizes the r-bit signal to a lower resolution, preferably with the r-bit input signal being received by the converter at the same rate as the s-bit output signal is generated.

On Page 3 of the specification, edit as follows:

Paragraph 1, line 1

The processor(s) and converter(s), which reduce the number of transmitted bits at the input to the interface in both the analog-to-digital and digital-to-analog chains, are preferably noise-shaping converters such as sigma-delta modulators. The quantization noise which results from the further quantization of the multi-bit digital signals, before the signals are transmitted across the interface, is shaped out of the band of interest.